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A new generation of detector controllers

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Abstract. During the period 1983-2001 three generations of detector controllers have been designed and built by the Detector Working Group (DWG). The last model built is a new controller able to drive both CCD and IR sensors.

Key words. CCD controller, IR detectors

1. Introduction

This paper will expose the last activities of the Detector Working Group (DWG) on the field of controllers compatible with CCD detectors (Charge Coupled Device) and for DRO detectors (Direct Readout). We will describe here the previously realized systems, pointing our attention on the controllers in use at the Telescopio Nazionale Galileo (TNG) and their main upgrades. In particular we will discuss:

- host-computer interface
- high speed communications link
- sequencer
- analogic signal processing

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2. Evolution of DWG detector controllers

A typical detector controller is composed by several subsystems based on different technologies. Some of these subsystems are common to different controller models, in particular:

- an host-computer interface
- communication links between host and detector subsystem
- a digital programmable sequencer
- a clock programmable generator
- a preamplifier
- An analog-signal processing and analog to digital conversion subsystem

The evolution, here described in the design of the later subsystems follows the three generations of detector controller developped by the DWG, namely, the systems mounted at the Asiago and Loiano Observatories (1983), the systems mounted at the TNG telescope (1994) and the last generation of detector controllers (CCDC-II).

All these systems are basically divided in two parts, a first one (local) near to the host computer and based on a standard bus (VME, VSB, PCI and CPCI) and a second one near to the detectors (remote). The two parts are interconnected by means of a digital link. The last generation makes use of a full-duplex link with a very high throughput (1.2 Gbaud) and with the following communication capabilities:

- transmission of clock sequences and commands (local to remote)
- transmission of data and telemetry (remote to local)

Due to the very high throughput of the link, all the intelligent parts (CPU, DSP) have been moved near the host computer, leaving near the detector only the analogic parts, more sensitive to noise coupling. In this way a resolution in generating clock phases, of about 50 nSec, is assured. Moreover the newest links (HP-HYPPY for example) allow to reshape the clock signal after the reception with advantages in reducing scan jitter and noise coupling to the analogic section.

As an example of second generation system Tab. 1 shows the main dynamic and electro-optical features of the Optical Imager Galileo (OIG) mounted at the TNG Nasmyth-A focus. The camera is based on a mosaic of two Marconi 2Kx4K CCDs.

The system shows a good readout noise, the total absence of cross talk between the video outputs but a readout time per pixel (18μSec/pixel) too high for the current standards. The reason of this limitation is concerned with:

- the analogic processor speed
- the A/D Crystal converter speed (10 μSec)
- the data link speed (20 Mbaud)

A complete revision of this system was then started two years ago producing the CCDC-II model.

3. The CCDC-II generation of controllers

In the design of the new system several points have been considered as mandatory:

1. fiber link with full-duplex high transmission speed (1.2 Gbaud, HP-HYPPY)
2. Increased number of input video channels
3. reduced sensitivity to electro-magnetic interference noise (EMI)
4. a more compact structure
5. capability to drive IR sensors
6. compatibility with standard bus architectures (PCI, CPCI, PMC)
7. reduced power dissipation

To satisfy items 1, 2, 6 and 7 some new functionalities have been introduced:

- a new sequencer based on the fast Motorola DSP56301 working on the host
- Interface board with DMA transfer based on PCI, CPCI or PMC bus standard
- low power 16 bit A/D converters without pipeline and with a conversion time of 500 nSec

Conversely item 5 required a new design for the architecture of the video-analogic section (see paragraph 5). Conversely some already optimized parts of the controller are basically unchanged, among them:

- programmable and buffered BIAS generators
- programmable and buffered Clock generators
- control and programmable temperature system
- shutter electronics
- telemetry electronics

Tab. 2 presents a complete summary of the characteristics of the controllers presented in this paper. To be noticed the possibility to operate directly on data coming from the detector (pixel scrambling, fast

parameter:	CCD #1	CCD #2
Conversion factor (e/ADU)	1.35	1.44
Readout noise (ADU-elecntrons)	3.3-4.45	2.6-3.7
Readout time (binn 1, output 2, seconds)	200	200
Readout time (binn 2, output 4, seconds)	100	100
Readout time (binn 2, output 2, seconds)	60	60
Readout time (binn 2, output 4, seconds)	30	30

Table 1. The main dynamic and electro-optical features of the Optical Imager Galileo (OIG) mounted at the TNG Nasmyth-A focus.

CCDC MODEL	ASIAGO CCDC 1983	TNG CCDC-I 1994	TNG CCDC-II 2000
Sequencer	Memory Wavetable	DSP 56001	DSP 56301
	Resol.: 2 μSec	Resol.: 100 nSec	Resol.: 40 nSec
Interface	VME	VME/VSB	PCI/CPCI
Data Link	Twisted pair	Fiber transputer	Fiber Gigalink
	harness	link 20 Mbaud	1.2 Gbaud
Clock	local	local	local
Data handling	MC68010	Transputer	Host processor
channels	1x (15 bit ADC)	2x4 (16 bit ADC)	8x4 (16 bit ADC)
Pixel Process.	Coor dual slope	Corr. dual slope	Corr. dual sampling
			single sampling
Prog. Biases	NN	2x8 (14 bi DAC)	8x16 (14 bit DAC)
Prog. Clocks	NN	2x8 (8 bit DAC)	8+8+8 (10 bit DAC)
Telemetry	Bias+Clock+Temp	Bias+Clock+Temp	Bias+Clock+Temp
Power supply	series regulation	series regulation	series regulation
Adj. offset	NN	Only out-offset	IN and OUT offset
CCD conv. factor	1 μV/e	4.7 μV/e	4.7 μV/e
CCD output Noise	7e @ 20μSec	4e @ 10μSec	4e @ 10μSec
		6e @ 2μSec	6e @ 2μSec
		6e @ 2μSec	6e @ 2μSec
Amplifier noise	0.3+0.4 μV (OPA27	4.5 μV (OPA627	1+2 μV (AD797
	@ 10 Khz, 10KΩ	@ 1 Mhz, 10KΩ	@ 1 Mhz, 10KΩ
Gain @ 1ADU/e	150	30	30

Table 2. Features and main differences among the three generations of controllers.

co-add, offset removal, etc.) as required by several applications directly with the host CPU via fast DMA transfer. In the older systems this possibility was obtained by dedicated hardware placed inside the controller.

4. Evolution of sequencers

As in the OIG controller, the new design of the sequencer is DSP based in particular we used the new Motorola DSP56301 model. This processor is compatible with the older 56001 so the software which generates the waveforms is basically unchanged. Fig 1 shows the evolution of sequencer systems. The first system implemented to generate complex sequences was based on the wavetables principle. Digital waveforms, composed by series of high and low states, were downloaded on RAM and then scanned cyclically by a programmable counter. This system is unefficient in that it requires the writing of a lot of states also when the output waveform is unchanged.

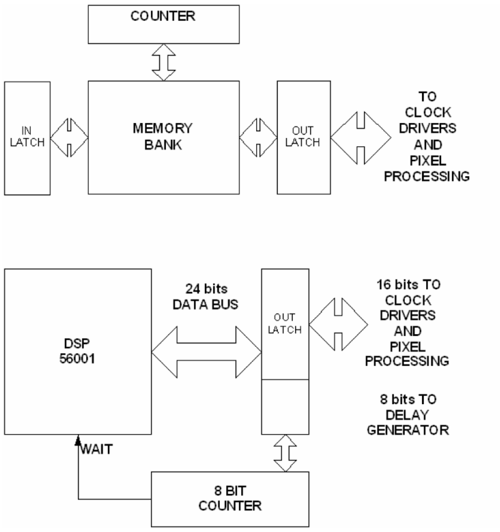

Fig. 1. Evolution of sequencer generators, on top wavetable system, below DSP sequencer.

Moreover this system suffers of flexibility for complex sequences. These problems have been resolved using a DSP allowing intelligent handling of compressed format tables. In the last sequencer a time resolution of 40 nSec per state has been reached with the DSP56301.

5. Evolution of processing and conversion electronics

In the case of CCD detector technology, the first processing level is made by:

- the subtraction of the reset pedestal with the associated fluctuations for each pixel
- the filtering to bandlimit the signal before digital conversion

The first step can be accomplished with several techniques. Fig. 2 shows the analytical result for a system based on an invertible discrete integrator (DSI, dual slope integrator).

The time diagram at the right is referred to pixel readout centered at the charge output. I+ indicates the first integral on the pedestal, while I- the one on the signal plus pedestal. The ouput of the DSI will be the results of two components (see Fig. 2 formula and Bode plot):

- the first part is a function of the integration time T (typically the ramping-rate of the integrator). This part characterizes the roll-over at high frequency
- the second part is a function of T and of the interval D between the two integrals. This part characterizes the low frequency profile and produces the "zero" of the transfer function at the origin

A different concept, the correlated double sampling CDS, is shown in Fig 3. Here a low-pass function is obtained in input with a bandpass filter (T_f time constant), while the derivative of the pedestals is obtained by two passive sample-holds followed by an OP-AMP differential stage. The behaviour in frequency is similar to the previous case of Fig. 2. The analytical function is made by a low-pass filter term and a high-pass filter term. The electronic implementation of such circuit is simpler, allows faster speeds and is suitable for IR detectors.

Examples of DSI and CDS electronic circuits are discussed in several papers, (see for example Bortoletto & D'Alessandro 1986) and Janesick (2000).

IR sensors are characterized by direct pixel non destructive readout. This is obtained via a row and column miltiplexer adressing each pixel both for instantaneous readout or reset.

Because of the absence of a coerent pedestal for each pixel and among all the pixels, noise and non-linearity may arise. They can be coherently subtracted only through indipendent readouts on the same pixel. So several readout strategies are possible: single-sampling, relative-sampling, correlated double sampling, correlated triple sampling (see Fig. 4) .

In Fig. 5 the CDS electronics design mounted on the new controller is shown.

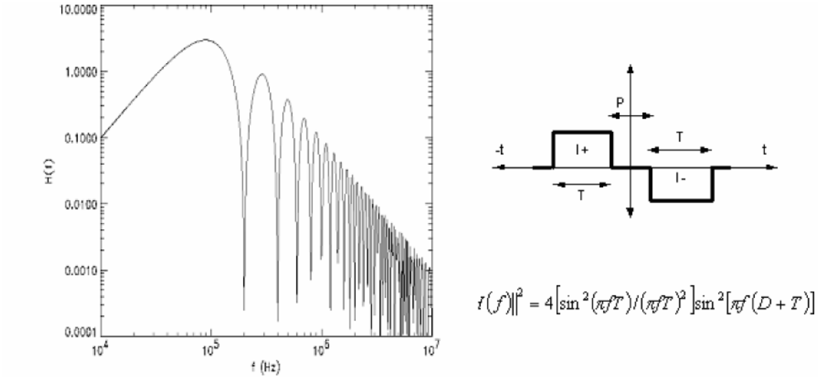

Fig. 2. Analytical representation of the dual slope integration (DSI) function

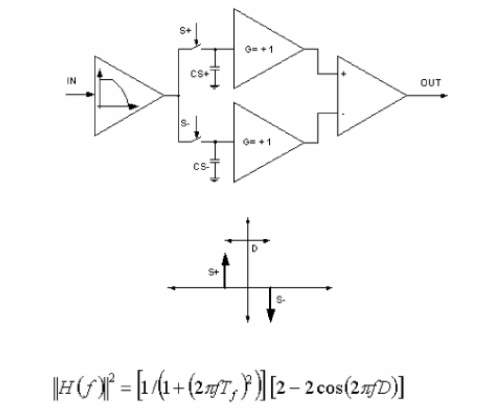

Fig. 3. Analytic function for the correlated double sampling (CDS)

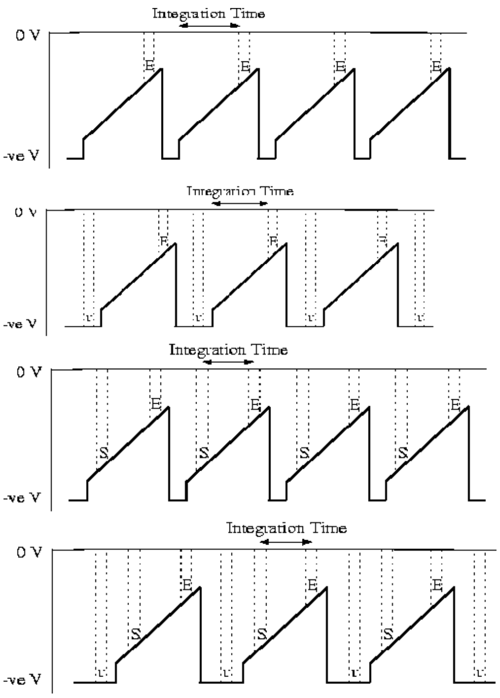

Fig. 4. Different IR sensors readout strategies, from top to bottom: single-sampling, relative-sampling, correlated double sampling, correlated triple sampling

One can see, on the left the differential preamplifier and the filtering section, while, on the right, the differential sampling section and the A/D converter are shown.

Two jumpers (S-SEL1, S-SEl2) permit to configure the CDS modality in the CCD case or a pseudo CDS modality used by IR sensors. Other improvements are:

– three different programmable gains of the input channels
– three programmable filtering high-cutoffs
– programmable offset at CDS input
– programmable offset at CDS output
– jumpering to select different references on the "dummy" channels of the input differential pre-amplifier

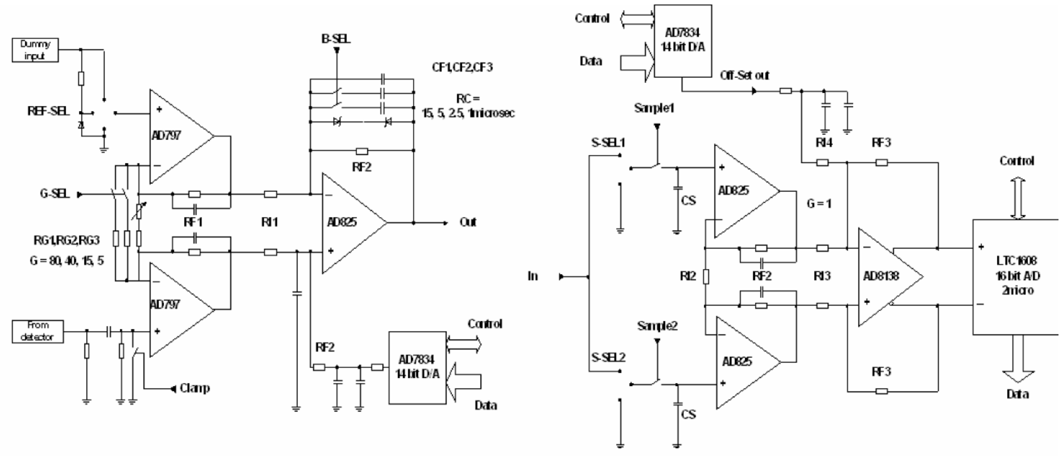

Fig. 5. The CDS processor of the new generation controller

6. Software

The new controller has been designed to be compatible with the previous control software. However the implementation of the system on PCI standard required the writing of a complete new driver. Marginal modifications are present in the following parts:

– ATV quick look based on IDL language (see Barth 2001, for details);
– off-line program for the generation of readout sequences based on Visual Basic language.

In the next future we will consider the possibility to write the user interface under JAVA environment and to write a new driver for WxWorks.

7. Development of the project and applications

At the present moment a complete prototype with PCI interface is ready. It will be tested with a CCD detector and with an InSb Raytheon 256x256 IR detector. This controller has been already tested with a PCI driver under Windows 2000. A new system with PMC interface and WxWorks driver is under design.

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