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Dedicated Hardware Devices for scientific applications

V. Rosato[1],[2]

[1] ENEA, Casaccia Research Center Computing and Modeling Unit (CAM),

[2] INFM, Istituto Nazionale di Fisica della Materia, Unita' di Ricerca Roma 1

Abstract. Dedicated harware devices are computational devices specifically projected to perform particular computational tasks. Astrophysics is one of the field where dedicated harware devices have found most successful applications. Here I briefly illustrate the generale characteristics of such devices, some of theri applications in astrophysics and related activity at ENEA Casaccia in Rome.

Key words. dedicated hardware–computational astrophysics

1. Dedicated hardware devices and astrophysics

Dedicated Hardware Devices (DHD hereafter) are custom devices, usually composed by silicon chips suitably designed and realized to perform, in the most efficient way, a specific computational task required by a given scientific application (Cleri et al. 2001). To cope with the high non-recurrent costs related to the use of ASIC technology, most of the DHD realized in a number of scientific domains have been implemented by using the FPGA (Field Programmable Gate Arrays) technology. FPGA are programmable silicon chips (to date technology allows to store about 10 millions equivalent gates in a FPGA) where the electronic circuit reproducing a given calculation can be mapped via software (no need of lithographic processes). This allows the use and reuse of the device in a number of different applications. The DHD option consists in the design of an electronic circuit, which performs the same computations of a given section (usually the most computationally demanding part) of a scientific code. The circuit is then implemented on a board containing the FPGA (plus memory banks) connected to a general-purpose platform (a PC, for instance), which acts as a host, via the PCI bus. This solution configures an "heterogeneous" computational platform characterized by the coexistence of a general-purpose platform (the PC cluster, for instance) and that of a DHD connected via the PCI bus. The FPGA-based DHD board acts as a booster which is activated, by the main code running on the general-purpose part of the platform, in the same way of a subroutine; differently from what would occur in a usual implementation, the section of the code mapped on the

Send offprint requests to: V. Rosato
Correspondence to: ENEA, Casaccia Research Center .O. Box 2400 0100 Roma

FPGA board is allotted for execution to the board itself. The code usually receives a formidable boost of computational power; the gain of perfomance might range from a few times up to hundred times with respect to that attainable, by the same code, on a general-purpose processor. The advantages of the DHD solution, over the ASIC technology, are related to a relevant reduction of the non-recurrent costs; moreover, FPGA can be programmed an unlimited number of times to "reproduce" different types of computations.

Computational Astrophysics has been among the scientific domains which firstly adhered to the DHD approach; the project GRAPE (GRAvitational PiPE) still remains one of the most successfull application of this approach in a computationally intense scientific domain (Makino et al. 1998). Fig.1 reports the architecture of the dedicated chip which constitutes the computational core of the GRAPE6 machine, allowing the full 2048 processors platform to attain 100 Tflops on MD codes of gravity/coulomb systems. In recent times, also bioinformatics [1], signal processing (David et al. 2002) and other scientific areas have greatly benefited of the increase of (cheap) computational power triggered by the design and the use of DHDs in the form of a part of "heterogeneous" computing machines.

The group of the Computing and Modeling Unit of ENEA has developped, in the last years, a software tool which allows to automatically design an electronic circuit, starting from the high-level implementation (a C code, for instance) of the computations which the circuit must perform (Marongiu & Palazzari 2000). The software tool, called PHG, maps a C code into a VHDL code which defines the optimum circuit "equivalent" to the C code, i.e. which performs the same operations on the input data (fig.2).

The PHG is able to autonomously extract the parallelism which is inherent to the high-level code and is able to give a (nearly) optimum solution for its hardware implementation, under the constraints given by the adopted technical solution (type of FPGA, number of equivalent gates available, total memory present in the board etc.). This allows to feed the silicon surface with a (usually large) number of functional units which perform the computational tasks in a way to otpimize the total computational effort.

The ENEA group is going to produce an industrial spin-off aimed at the deployment of the PHG and its use for the design of DHD in several scientific areas. Among the areas which could receive substantial benefits from the DHD approach we can quote bioinformatics, signal and image processing. The actual characteristics of FPGA technology do not allow to efficiently cope with complex floiting point operations. However, the same "concept" of DHD can be adopted on different technological supports; FPGA can be substituted with DSP (Digital Signal Processing)-based board which, in turn, may host complex floating point operations with (actual) performances reaching up to about 10 Gflops per board. A very interesting property related to the DHD technology is related to the fact that the hardware design can be kept constant while the physical properties of the technological support might constantly improve; the same electronic circuit, for instance, will be implemented on next generation FPGA-based boards very easily; this will allow to increase the DHD performance, at least, by a factor equal to the clock frequency ratio. The availability of a larger silicon area, on next generation FPGAs, will allow to feed the device with larger and larger parts of the code, thus allowing the increase of the overall efficiency of the adopted DHD solution.

[1] see the web pages www.timelogic.com and www.paracel.com. These two companies have as a major technological asset the realization of dedicated platforms which boost the computational tasks of sequence analysis.

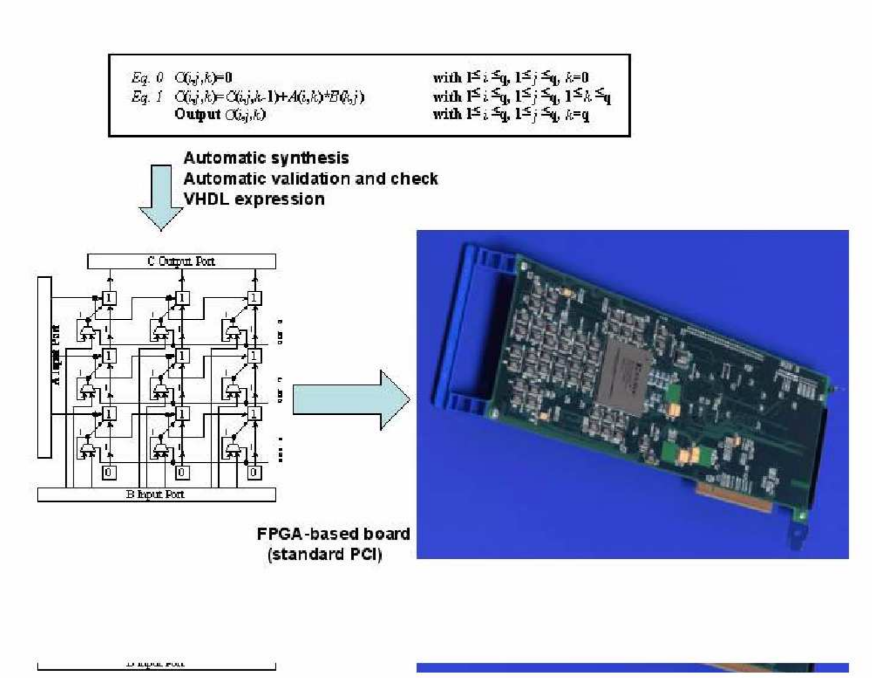

Fig. 1. Architecture of the GRAPE6 chip designed to power the GRAPE6 machine $(http://grape.astron.s.utokyo.ac.jp/\ makino/talks/mirai_symp2002/lpage_14.html$

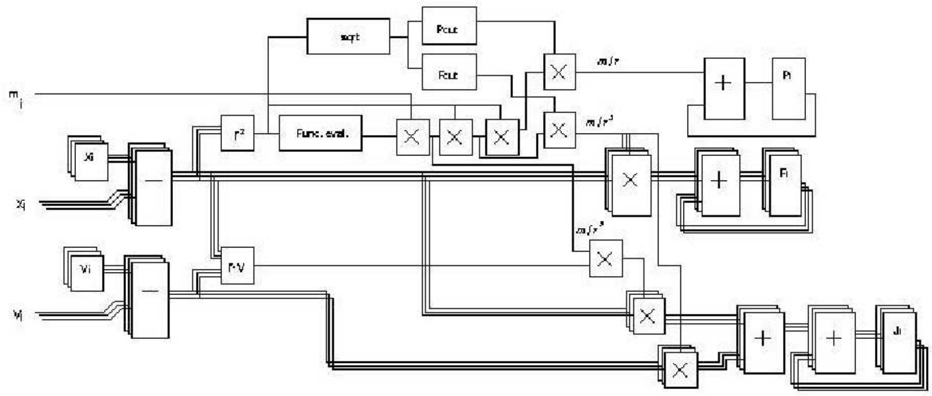

Fig. 2. Conceptual action of the PHG (Parallel Hardware Generator): the high-level code is transformed into a VHDL code (which expresses the feature of the circuit) which is then implemented (via the usual EDA tools) on the FPGA-based board, which is connected to the host via the PCI bus.

The ENEA group wishes to collaborate with all the scientific groups whose computational tasks might be suitably mapped onto a DHD platform. The automatic synthesis of a VHDL code from the C code allows to rapidly prototyping a DHD device, thus allowing a rapid evaluation of the cost/benefits ratio of the solution.

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